ABSTRACT OF DISCLOSURE

A semiconductor device, and method for manufacturing the same, manufactured by a simpler process, compared to a conventional trench lateral power MOSFET for a withstand voltage of 80 V, having a smaller device pitch and lower on-resistance per unit area as compared with a conventional lateral power MOSFET with a withstand voltage lower than 80 V. The semiconductor device may include a shallow and narrow trench formed in a substrate with small spacing, a drift region that is an n diffusion region formed around the trench, a gate oxide film having a uniform thickness of about 0.05 μ m formed inside the trench, a gate polysilicon formed inside the gate oxide film, a base region and a source region that is an n^+ diffusion region formed in the surface region of the substrate, a drain region that is an n^+ diffusion region formed at the trench bottom, interlayer dielectric provided inside the gate polysilicon, and drain polysilicon filling a space inside the interlayer dielectric in the trench and electrically connecting to the drain region.